LISTING OF CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application.

Please amend claims 17, 24, 25 and 27, and add new claims 33-37 as follows.

Claims 1-16 (canceled)

17. (Currently amended) An electronic timepiece allowing ~~the~~ display of at least a first time related data item and a second time related data item, said first time related data item, being based on the Hour-Minute-Second~~Hour-Minute-Second~~ system, is displayed by a display, this timepiece including:

a time base supplying pulses to a frequency divider circuit including N binary division stages, wherein the frequency divider circuit is arranged to~~and~~ supply~~ying~~ first control pulses allowing said first time related data item to be formed and displayed by the display;~~,~~ and ~~this timepiece further including~~

generating means arranged to supply, from auxiliary control pulses originating from said time base, second control pulses allowing said second time related data item to be formed and displayed by the display,

wherein said second time related data item is based on a decimal system in which ~~the~~ time is divided at least into thousandths of a day and wherein said second time related data item is displayed with three digits so that said second time related data item~~it~~ cannot be confused with said first time related data item.

18. (Previously presented) The electronic timepiece according to claim 17, wherein said generating means are arranged to count successively the auxiliary control pulses in accordance with a counting sequence formed of counting operations of n and n+1 auxiliary control pulses succeeding each other in accordance with a determined order so that said generating means supply the second control pulses at a mean frequency allowing said second time related data item based on the decimal system to be formed, n being an integer number directly less than the division ratio of the frequency of said auxiliary control pulses by the frequency of said second control pulses.

19. (Previously presented) The electronic timepiece according to claim 18, wherein said counting operations of n and n+1 auxiliary control pulses follow each other in accordance with an order determined so that the second control pulses are supplied with minimum time error.

20. (Previously presented) The electronic timepiece according to claim 18, wherein said counting sequence is comprised in a table including as many entries as there are counting operations.

21. (Previously presented) The electronic timepiece according to claim 20, wherein said table is formed of a binary word in which the binary value « 0 » indicates that n auxiliary control pulses must be counted and the binary value « 1 » indicates that n+1 auxiliary control pulses must be counted.

22. (Previously presented) The electronic timepiece according to claim 20, wherein the entries of said table are indexed by means of a register containing a value of said second time related data item.

23. (Previously presented) The electronic timepiece according to claim 18, wherein said counting operations of n or n+1 auxiliary control pulses are determined by means of a register containing a value of said second time related data item.

24. (Currently amended) The electronic timepiece according to claim 17, wherein said generating means include a primary counter arranged for counting n auxiliary control pulses, and inhibition means for said primary counter arranged for periodically inhibiting k auxiliary control pulses upstream of said primary counter, so that the primary counter~~latter~~ supplies the second control pulses at a mean frequency allowing said second time related data item based on the decimal system to be formed, n being an integer number directly less than the division ratio of the frequency of said auxiliary control pulses by the frequency of said second control pulses.

25. (Currently amended) The electronic timepiece according to claim 24, wherein said inhibition means include a secondary counter arranged for counting m auxiliary control pulses, a logic detection circuit coupled to said secondary counter so as to detect k intermediate states thereof, and an AND logic gate including two inputs, one input being inverted and connected to an output of said logic detection circuit and

the other input receiving said auxiliary control pulses, wherein said logic detection circuit sends~~ing~~ an inhibition signal blocking the AND logic gate when one of the k intermediate states is detected~~,~~ so that one auxiliary control pulse is inhibited upstream of said primary counter.

26. (Previously presented) The electronic timepiece according to claim 25, wherein said k intermediate states are selected so as to be equidistant from each other.

27. (Currently amended) The electronic timepiece according to claim 17, wherein said generating means include a primary counter arranged for counting n+1 auxiliary control pulses, and initialization means coupled to said primary counter and arranged for periodically initializing said primary counter with a value k corresponding to a complementary number of auxiliary control pulses so that said primary counter supplies the second control pulses at a mean frequency allowing said second time related data item based on the decimal system to be formed, wherein n+1 is~~being~~ an integer number directly greater than the division ratio of the frequency of said auxiliary control pulses by the frequency of said second control pulses.

28. (Previously presented) The electronic timepiece according to claim 27, wherein said initialization means include a secondary counter arranged for counting m second control pulses and an initialization circuit coupled to said primary counter, said secondary counter providing a signal to said initialization circuit every m second control pulses so that said primary counter is initialized with a value k.

29. (Previously presented) The electronic timepiece according to claim 17, wherein said auxiliary control pulses are supplied at an output of one of the binary division stages of said frequency divider circuit.

30. (Previously presented) The electronic timepiece according to claim 17, wherein said auxiliary control pulses are supplied at an output of N* additional binary division stages connected after said frequency divider circuit upstream of said generating means.

31. (Previously presented) The electronic timepiece according to claim 17, wherein said generating means supply said second control pulses at a mean frequency of 1/8.64 Hz.

32. (Previously presented) The electronic timepiece according to claim 17, wherein said generating means supply said second control pulses at a mean frequency of 1/86.4 Hz.

33. (NEW) The electronic timepiece according to claim 17, wherein the first time related data item is based on the Hour-Minute-Second system that consists of dividing a day into 24 hours, with 1 hour being divided into 60 minutes, and with 1 minute being divided into 60 seconds.

34. (NEW) The electronic timepiece according to claim 17, wherein the second time related data item is based on the decimal system that consists of dividing a day into 10 tenths of a day, with each tenth of a day being divided into 10 hundredths of a day, and with each hundredth of a day being divided into 10 thousandths of a day.

35. (NEW) The electronic timepiece according to claim 17, wherein the display includes a first display and a second display, and the first display displays the first time related data item and the second display displays the second time related data item.

36. (NEW) The electronic timepiece according to claim 35, wherein the first display includes either four digits or first and second hands.

37. (NEW) An electronic universal timepiece allowing display of at least a first time related data item and a second time related data item, the first time related data item, being based on the Hour-Minute-Second system that consists of dividing a day into 24 hours, with 1 hour being divided into 60 minutes, and with 1 minute being divided into 60 seconds, is displayed by a display, the timepiece comprising:

a time base supplying pulses to a frequency divider circuit, the frequency divider circuit including N binary division stages, wherein the frequency divider circuit is arranged to supply first control pulses allowing the first time related data item to be formed and displayed by the display; and

generating means arranged to supply, from auxiliary control pulses originating from the time base, second control pulses allowing the second time related data item to be formed and displayed by the display;

wherein the first time related data item is formed and displayed by the display as hours and minutes, either with four digits or first and second hands for displaying hours and minutes in the Hour-Minute-Second system;

wherein the second time related data item is based on a decimal system that consists of dividing a day into 10 tenths of a day, with each tenth of a day being divided into 10 hundredths of a day, and with each hundredth of a day being divided into 10 thousandths of a day, and

wherein the second time related data item is displayed by the display in the decimal system as tenths, hundredths and thousandths of a day with three digits.